

# **Digital Logic & Computer Organization and Architecture**

**(Code : CSC304)**

**Semester III – Computer Engineering / Computer Science and Engineering / Artificial Intelligence and Data Science/ Machine Learning/ Cyber Security/ Internet of Things(IoT) / Data Engineering / Data science Internet of Things and Cyber Security Including Block Chain Technology**

(Mumbai University)

**Strictly as per New Choice Based Credit and Grading System Syllabus  
(Revise 2019 'C' Scheme) of Mumbai University with effective from Academic Year 2020-2021**

**J. S. Katre**

M.E. (Electronics and Telecommunication)  
Formerly, Assistant Professor  
Department of Electronics Engineering  
Vishwakarma Institute of Technology (V.I.T.), Pune.  
Maharashtra, India

**Harish G. Narula**

Formerly Assistant Professor (Senior)  
Department of Computer Engineering  
D. J. Sanghvi College of Engineering, Mumbai.  
Maharashtra, India.



**TechKnowledge<sup>TM</sup>**  
Publications

(Book Code : MO147B)



**Digital Logic & Computer Organization and Architecture (Code : CSC304)**

(Semester III, Computer Engineering / Computer Science and Engineering / Artificial Intelligence and Data Science/ Machine Learning/ Cyber Security/ Internet of Things(IoT) / Data Engineering / Data science Internet of Things and Cyber Security Including Block Chain Technology, Mumbai University)

J. S. Katre, Harish G. Narula

Copyright © Authors. All rights reserved. No part of this publication may be reproduced, copied, or stored in a retrieval system, distributed or transmitted in any form or by any means, including photocopy, recording, or other electronic or mechanical methods, without the prior written permission of the publisher.

This book is sold subject to the condition that it shall not, by the way of trade or otherwise, be lent, resold, hired out, or otherwise circulated without the publisher's prior written consent in any form of binding or cover other than which it is published and without a similar condition including this condition being imposed on the subsequent purchaser and without limiting the rights under copyright reserved above.

**First Printed in India** : January 2002

**First Edition** : August 2020 (**TechKnowledge Publications**)

**Second Revised Edition** : June 2021

This edition is for sale in India, Bangladesh, Bhutan, Maldives, Nepal, Pakistan, Sri Lanka and designated countries in South-East Asia. Sale and purchase of this book outside of these countries is unauthorized by the publisher.

**ISBN :** 978-81-947407-5-9

**Published by :**

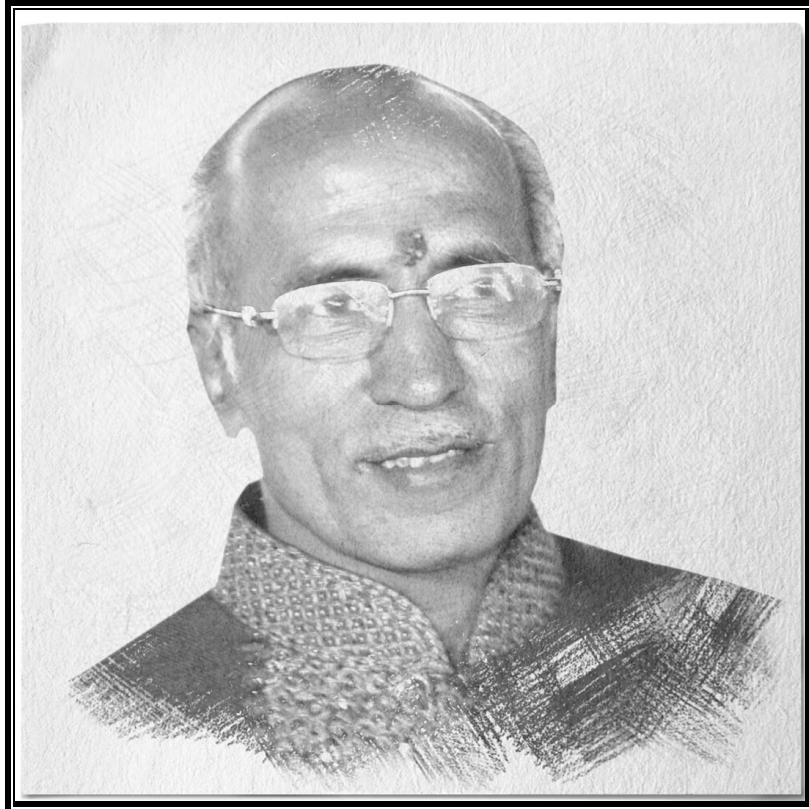
**TechKnowledge Publications**

**Head Office :** B/5, First floor, Maniratna Complex, Taware Colony, Aranyeshwar Corner,  
Pune - 411 009. Maharashtra State, India  
Ph : 91-20-24221234, 91-20-24225678.  
Email : [info@techknowledgebooks.com](mailto:info@techknowledgebooks.com),  
Website : [www.techknowledgebooks.com](http://www.techknowledgebooks.com)

[CSC304] (FID : MO147) (Book Code : MO147B)

(Book Code : MO147B)

*We dedicate this Publication soulfully and wholeheartedly,  
in loving memory of our beloved founder director,  
Late Shri. Pradeepji Lalchandji Lunawat,  
who will always be an inspiration, a positive force and strong support  
behind us.*



*“My work is my prayer to God”*

*- Lt. Shri. Pradeepji L. Lunawat*

*Soulful Tribute and Gratitude for all Your  
Sacrifices, Hardwork and 40 years of Strong Vision...*

## Syllabus...

**DLCO&A : Sem. III, CE / CSE / AI and Data Science/ Machine Learning/ Cyber Security/ IoT / Data Engg. / Data science IoT and Cyber Security Including Block Chain Technology (MU)**

Course Code	Course Name	Credit
CSC304	Digital Logic & Computer Organization and Architecture	3

**Pre-requisite :** Knowledge on number systems

**Course Objectives :**

1. To have the rough understanding of the basic structure and operation of basic digital circuits and digital computer.
2. To discuss in detail arithmetic operations in digital system.
3. To discuss generation of control signals and different ways of communication with I/O devices.
4. To study the hierarchical memory and principles of advanced computing.

**Course Outcome :**

1. To learn different number systems and basic structure of computer system.
2. To demonstrate the arithmetic algorithms.
3. To understand the basic concepts of digital components and processor organization.
4. To understand the generation of control signals of computer.
5. To demonstrate the memory organization.
6. To describe the concepts of parallel processing and different Buses.

## **Module 1**

### **Computer Fundamentals :**

Introduction to Number System and Codes Number Systems: Binary, Octal, Decimal, Hexadecimal, Codes: Grey, BCD, Excess-3, ASCII, Boolean Algebra. Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR, Overview of computer organization and architecture. Basic Organization of Computer and Block Level functional Units, Von- Neumann Model.

**(Refer chapter 1)**

## **Module 2**

### **Data Representation and Arithmetic algorithms :**

Binary Arithmetic: Addition, Subtraction, Multiplication, Division using Sign Magnitude, 1's and 2's compliment, BCD and Hex Arithmetic Operation. Booths Multiplication Algorithm, Restoring and Non-restoring Division Algorithm. IEEE-754 Floating point Representation.

**(Refer chapter 2)**

## **Module 3**

### **Processor Organization and Architecture :**

Introduction: Half adder, Full adder, MUX, DMUX, Encoder, Decoder(IC level). Introduction to Flip Flop: SR, JK, D, T (Truth table). Register Organization, Instruction Formats, Addressing modes, Instruction Cycle, Interpretation and sequencing.

**(Refer chapter 3)**

## **Module 4**

### **Control Unit Design :**

Hardwired Control Unit: State Table Method, Delay Element Methods. Microprogrammed Control Unit: Micro Instruction-Format, Sequencing and execution, Micro operations, Examples of microprograms.

**(Refer chapter 4)**

## **Module 5**

### **Memory Organization :**

Introduction and characteristics of memory, Types of RAM and ROM, Memory Hierarchy, 2-level Memory Characteristic, Cache Memory: Concept, locality of reference, Design problems based on mapping techniques, Cache coherence and write policies. Interleaved and Associative Memory.

**(Refer chapter 5)**

## **Module 6**

### **Principles of Advanced Processor and Buses :**

Basic Pipelined Data path and control, data dependencies, data hazards, branch hazards, delayed branch, and branch prediction, Performance measures-CPI, Speedup, Efficiency, throughput, Amdhal's law. Flynn's Classification, Introduction to multicore architecture. Introduction to buses: ISA, PCI, USB. Bus Contention and Arbitration.

**(Refer chapter 6)**



**Module 1****Chapter 1 : Computer Fundamentals 1-1 to 1-58**

**Syllabus :** Introduction to number system and codes, Number systems : Binary, Octal, Decimal, Hexadecimal, Codes : Gray, BCD, Excess-3, ASCII, Boolean algebra, Logic gates : AND, OR, NOT, NAND, NOR, EX-OR, Overview of computer organization and architecture, Basic organization of computer and block level functional units, Von-Neumann model.

1.1	Introduction .....	1-2
1.2	System or Circuit .....	1-2
1.2.1	Analog Systems .....	1-2
1.2.2	Digital Systems .....	1-2
1.3	Number Systems .....	1-2
1.3.1	Important Definitions Related to All Numbering Systems .....	1-2
1.3.2	Various Numbering Systems .....	1-3
1.4	The Decimal Number System .....	1-3
1.4.1	Characteristics of a Decimal System .....	1-3
1.5	The Binary Number System .....	1-4
1.5.1	Characteristics of a Binary System .....	1-4
1.5.2	Binary Number Formats .....	1-4
1.6	Octal Number System .....	1-5
1.6.1	Binary Coded Octal (BCO) .....	1-5
1.7	Hexadecimal Number System .....	1-5
1.8	Counting in a General Radix (Base) r .....	1-6
1.9	Conversion of Number Systems .....	1-7
1.9.1	Conversion from Binary, Octal or Hex to Decimal .....	1-7
1.9.2	Conversion from Decimal to Binary, Octal or Hex .....	1-8
1.9.3	Binary to Octal Conversion .....	1-16
1.9.4	Binary to Hex Conversion .....	1-16
1.9.5	Octal to Binary Conversion .....	1-16
1.9.6	Hex to Binary Conversion .....	1-17
1.9.7	Octal to Hex Conversion .....	1-17

1.9.8	Hex to Octal Conversion .....	1-17
1.10	Concept of Coding .....	1-20
1.10.1	Applications of Binary Codes .....	1-20
1.11	Classification of Codes .....	1-20
1.11.1	Weighted Binary Codes .....	1-20
1.11.2	Non-Weighted Codes .....	1-21
1.11.3	Reflective Codes .....	1-21
1.11.4	Sequential Codes .....	1-21
1.11.5	Alphanumeric Codes .....	1-21
1.11.6	Error Detecting and Correcting Codes .....	1-21
1.12	Binary Coded Decimal (BCD) Code .....	1-21
1.12.1	Conversion from Decimal to BCD .....	1-22
1.12.2	Comparison with Binary .....	1-22
1.13	Non – weighted Codes .....	1-23
1.13.1	Excess – 3 Code .....	1-23
1.14	Gray Code .....	1-24
1.14.1	Application of Gray Code .....	1-24
1.14.2	Advantages of Gray Code .....	1-24
1.14.3	Gray-to-Binary Conversion .....	1-24
1.14.4	Binary to Gray Conversion .....	1-25
1.15	Alphanumeric Codes .....	1-26
1.15.1	ASCII - (American Standard Code for Information Interchange) .....	1-26
1.15.2	Extended ASCII Characters .....	1-27
1.16	Introduction to Boolean Algebra .....	1-29
1.16.1	Basic Logical Operations (Logic Variables) .....	1-29
1.16.2	Logic Gates .....	1-29
1.16.3	Gates, Symbols and Boolean Expression .....	1-29
1.17	Basic Definitions .....	1-29
1.17.1	Postulates .....	1-30
1.18	Axiomatic Definition of Boolean (Binary) Algebra .....	1-31
1.18.1	Boolean Postulates and Laws .....	1-31



1.19	Two Valued Boolean Algebra .....	1-32	1.30	Evolution of Computers .....	1-52
1.20	Basic Theorems and Properties of Boolean Algebra .....	1-33	1.30.1	Mechanical Era (160s-1940s) .....	1-52
	1.20.1 Duality .....	1-33	1.30.2	The Electronic Era .....	1-52
	1.20.2 Basic Theorems .....	1-33	1.31	Von Neumann and Harvard Architecture .....	1-54
	1.20.3 De-Morgan's Theorems .....	1-35	1.31.1	Von Neumann Architecture .....	1-54
1.21	Boolean Expression and Boolean Function .....	1-36	1.31.2	Harvard Architecture .....	1-57
	1.21.1 Truth Table Formation .....	1-36	•	<b>Review Questions .....</b>	<b>1-57</b>
	1.21.2 Examples on Reducing the Boolean Expression .....	1-36	<b>Module 2</b>		
	1.21.3 Complement of a Function .....	1-39	<b>Chapter 2 : Data Representation and Arithmetic Algorithms</b> <b>2-1 to 2-50</b>		
1.22	Logic Gates .....	1-40	<b>Syllabus :</b> Binary arithmetic : Addition, Subtraction, Multiplication, Division using sign magnitude, 1's and 2's compliment, BCD and Hex arithmetic operation, Booths multiplication algorithm, Restoring and non-restoring division algorithm, IEEE-754 floating point representation.		
	1.22.1 Classification of Logic Gates .....	1-40	2.1	Unsigned Binary Numbers .....	2-2
1.23	NOT Gate or Inverter .....	1-40	2.1.1	Important Features of Unsigned Numbers .....	2-2
1.24	AND Gate .....	1-40	2.2	Binary Arithmetic of Unsigned Numbers .....	2-2
1.25	The OR Gate .....	1-41	2.2.1	Binary Addition .....	2-2
1.26	Special Type of Gates or Derived Gates .....	1-41	2.2.2	Sum and Carry .....	2-3
	1.26.1 The EX-OR Gate .....	1-41	2.2.3	Addition of Large Binary Numbers .....	2-3
	1.26.2 The EX-NOR Gate .....	1-41	2.2.4	Binary Subtraction .....	2-3
	1.26.3 Realization of Switching Functions .....	1-42	2.2.5	Subtraction and Borrow .....	2-3
	1.26.4 To Draw a Logic Circuit from Boolean Equation .....	1-42	2.2.6	Subtraction of Larger Binary Numbers .....	2-3
	1.26.5 To Write a Boolean Expression for a Logic Circuit .....	1-43	2.2.7	Binary Multiplication .....	2-4
1.27	Universal Gates .....	1-44	2.2.8	Binary Division .....	2-4
	1.27.1 The NAND Gate .....	1-44	2.3	Sign-Magnitude Numbers .....	2-5
	1.27.2 Universality of NAND Gate .....	1-45	2.3.1	Range of Sign-Magnitude Numbers .....	2-5
	1.27.3 The NOR Gate .....	1-46	2.4	Complements .....	2-6
	1.27.4 Universality of NOR Gate .....	1-46	2.4.1	Types of Complements .....	2-6
	1.27.5 Solved Examples .....	1-48	2.4.2	1's Complement .....	2-6
1.28	Introduction to Computer Organization .....	1-50	2.4.3	2's Complement .....	2-7
1.29	Basic Organization of Computer and Block Level Description of Functional Units .....	1-51	2.5	Binary Subtraction using 1's and 2's Complements .....	2-7
	1.29.1 Structural Components of a Computer .....	1-51	2.5.1	Subtraction using 1's Complement .....	2-7
	1.29.2 Functional View of a Computer .....	1-52			



2.5.2	Binary Subtraction using 2's Complement Method .....	2-8	2.10.1	Restoring Division Method .....	2-36
2.6	Octal Arithmetic .....	2-12	2.11	Division of Integers : Non-restoring Method .....	2-41
2.6.1	Octal Addition .....	2-12	2.12	Floating Point Representation .....	2-43
2.6.2	Subtraction of Octal Numbers .....	2-12	2.12.1	IEEE-754 Standard for Representing Floating Point Numbers.....	2-45
2.6.3	Method 1 : Direct Subtraction of Octal Numbers .....	2-13	2.13	Floating Point Arithmetic : Addition, Subtraction, Multiplication, Division .....	2-48
2.6.4	Method 2 : Subtraction using 7's Complement .....	2-13	2.13.1	Multiplication .....	2-49
2.6.5	Method 3 : Subtraction using 8's Complement .....	2-14	2.13.2	Division .....	2-50
2.6.6	Octal Multiplication .....	2-15	•	<b>Review Questions .....</b>	<b>2-50</b>
2.6.7	Octal Division .....	2-16	<b>Module 3</b>		
2.7	Hexadecimal Arithmetic .....	2-16	<b>Chapter 3 : Processor Organization and Architecture</b>		
2.7.1	Hex Addition .....	2-16	<b>3-1 to 3-76</b>		
2.7.2	Hex Subtraction .....	2-17			
2.7.3	Method 1 : Direct Subtraction .....	2-17	<b>Syllabus :</b> Introduction : Half adder, Full adder, MUX, DMUX, Encoder, Decoder (IC level), Introduction to Flip Flop : SR, JK, D, T (Truth table), Register organization, Instruction formats, Addressing modes, Instruction cycle, Interpretation and sequencing.		
2.7.4	Hex Subtraction using 15's Complement .....	2-19			
2.7.5	Hex Subtraction using 16's Complement .....	2-20	3.1	Introduction .....	3-2
2.7.6	Hexadecimal Multiplication .....	2-21	3.1.1	Combinational Circuits .....	3-2
2.7.7	Hex Division .....	2-21	3.1.2	Sequential Circuits .....	3-2
2.8	BCD Arithmetic .....	2-22	3.1.3	Clock Signal .....	3-3
2.8.1	BCD Addition .....	2-22	3.1.4	Comparison of Combinational and Sequential Circuits .....	3-3
2.8.2	BCD Subtraction .....	2-24	3.1.5	Analysis of a Combinational Circuit .....	3-3
2.9	Integer Data Computation : Addition, Subtraction .....	2-27	3.1.6	Design of Combinational Logic using Statements .....	3-4
2.9.1	Integer Addition and Subtraction .....	2-27	3.2	Binary Adders .....	3-9
2.9.2	Multiplication : Unsigned Multiplication .....	2-27	3.2.1	Types of Binary Adders .....	3-9
2.9.3	Multiplication : Signed Multiplication Booth's Algorithm .....	2-29	3.2.2	Half Adder .....	3-9
2.9.4	Bit-pair Recoding of Multipliers (A Fast Multiplication Method) .....	2-35	3.2.3	Full Adder .....	3-10
2.9.5	Hardware Implementation of Booth Algorithm .....	2-36	3.2.4	Full Adder using Half Adder .....	3-11
2.10	Division of Integers : Restoring Method .....	2-36	3.2.5	Applications of Full Adder .....	3-12
			3.2.6	Binary Subtractors .....	3-12
			3.2.7	Half Subtractor .....	3-12



3.2.8	Full Subtractor .....	3-13
3.3	The n-Bit Parallel Adder .....	3-14
3.3.1	A Four Bit Parallel Adder Using Full Adders .....	3-15
3.3.2	Propagation Delay in Parallel Adder ....	3-15
3.3.3	Look Ahead – Carry Adder .....	3-15
3.3.4	Four Bit Fast Adder with Look-Ahead Carry .....	3-17
3.3.5	Binary Adder IC 74 LS 83 / 74 LS 283 .	3-17
3.3.6	Four Bit Binary Adder using IC 7483 ....	3-18
3.3.7	Cascading of Adders .....	3-18
3.4	n-bit Parallel Subtractor .....	3-18
3.4.1	4 Bit Parallel Subtractor using IC7483 .	3-18
3.4.2	4-Bit Binary Parallel Adder/Subtractor Using IC 7483 .....	3-19
3.5	Multiplexer (Data Selector) .....	3-19
3.5.1	Necessity of Multiplexers .....	3-20
3.5.2	Advantages of Multiplexers .....	3-20
3.6	Types of Multiplexers .....	3-21
3.6.1	2 : 1 Multiplexer .....	3-21
3.6.2	A 4 : 1 Multiplexer .....	3-21
3.6.3	8 : 1 Multiplexer .....	3-22
3.6.4	16 : 1 MUX .....	3-22
3.7	Study of Different Multiplexer ICs .....	3-22
3.7.1	8 : 1 Multiplexer (74151) .....	3-23
3.7.2	54LS 153/DM 54LS 153/DM 74LS 153 (Dual 4 : 1 Multiplexer) .....	3-23
3.8	Multiplexer Tree / Cascading of Multiplexer .....	3-24
3.9	Use of Multiplexers in Combinational Logic Design .....	3-26
3.9.1	Implementation of a Logical Expression in the Standard SOP Form .....	3-26
3.9.2	Use of 8 : 1 MUX to Realize a 4 Variable Function .....	3-28
3.9.3	Implementation of a Logical Expression in the Non-standard SOP Form .....	3-33
3.9.4	Implementing a Standard POS Expression using Multiplexer .....	3-34
3.9.5	Implementation of Boolean SOP Expression with Don't Care Conditions .....	3-35
3.10	Demultiplexers .....	3-36
3.10.1	Demultiplexer Principle .....	3-36
3.11	Types of Demultiplexers .....	3-36
3.11.1	1 : 2 Demultiplexer .....	3-37
3.11.2	1 : 4 Demultiplexer .....	3-37
3.11.3	1 : 8 Demultiplexer .....	3-38
3.11.4	IC 74138 as 1 : 8 DE-MUX .....	3-38
3.11.5	1 : 16 Demultiplexer .....	3-39
3.11.6	DM 54 LS 154 / DM 74 LS 154 : 4 Line to 16 Line Decoder / Demux .....	3-39
3.12	Demultiplexer Tree .....	3-40
3.12.1	Use of DEMUX in Combinational Logic Design .....	3-42
3.13	Encoders .....	3-44
3.13.1	Types of Encoders .....	3-44
3.14	Priority Encoder .....	3-44
3.14.1	Priority Encoders in the IC Form .....	3-45
3.14.2	Octal to Binary Encoder .....	3-45
3.14.3	Decimal to BCD Encoder MSI IC 74147 .....	3-46
3.15	Decoder .....	3-46
3.15.1	2 to 4 Line Decoder .....	3-47
3.15.2	Demultiplexer as Decoder .....	3-47
3.15.3	3 to 8 Line Decoder .....	3-47
3.15.4	1 : 8 DEMUX as 3:8 Decoder .....	3-48
3.15.5	IC 74138 as 3 : 8 Decoder .....	3-48
3.15.6	4 Line to 16 Line Decoder using 3 : 8 Decoder .....	3-49
3.15.7	Combinational Logic Design Using Decoders .....	3-49
3.15.8	Advantage of Decoder Realization .....	3-53
3.16	Latches and Flip-flop .....	3-53



3.17	S-R Latch using NAND Gates .....	3-53
3.18	Triggering Methods .....	3-54
3.18.1	Concept of Level Triggering .....	3-54
3.18.2	Types of Level Triggered Flip-flops .....	3-55
3.18.3	Concept of Edge Triggering .....	3-55
3.18.4	Types of Edge Triggered Flip Flops .....	3-55
3.19	Edge Triggered S-R Flip-Flop .....	3-55
3.19.1	Positive Edge Triggered S-R Flip Flop ..	3-55
3.19.2	Negative Edge Triggered S-R Flip Flop ..	3-57
3.20	Edge Triggered D Flip Flop .....	3-57
3.20.1	Positive Edge Triggered D Flip Flop ..	3-57
3.20.2	Negative Edge Triggered D Flip Flop ..	3-58
3.21	Edge Triggered J-K Flip Flop .....	3-59
3.21.1	Positive Edge Triggered JK Flip Flop ..	3-59
3.21.2	Negative Edge Triggered JK flip-flop ..	3-60
3.22	Toggle Flip Flop (T Flip Flop) .....	3-61
3.22.1	Positive Edge Triggered T-FF .....	3-61
3.22.2	Negative Edge Triggered T Flip Flop ..	3-62
3.22.3	Application of T F/F .....	3-62
3.23	CPU Architecture and Register Organization .....	3-62
3.23.1	Instruction Formats .....	3-63
3.23.2	Instruction Word Format - Number of Addresses .....	3-64
3.23.3	Reverse Polish Notation .....	3-65
3.23.4	Basic Instruction Cycle .....	3-66
3.23.5	Interrupt Cycle .....	3-66
3.24	Addressing Modes .....	3-68
3.24.1	Examples on Addressing Modes .....	3-71
3.25	Instruction Interpretation and Sequencing and Micro-Operations with their Sequencing .....	3-71
3.25.1	Fetch Cycle .....	3-72
3.25.2	Execute Cycle .....	3-73
3.25.3	Interrupt Cycle .....	3-74
3.25.4	Applications of Microprogramming .....	3-74
•	Review Questions .....	3-75

**Module 4****Chapter 4 : Control Unit Design****4-1 to 4-16**

**Syllabus :** Hardwired control unit : State table method, Delay element methods, Microprogrammed control unit : Micro instruction-format, Sequencing and execution, Micro operations, Examples of microprograms.

4.1	CPU Architecture and Register Organization .....	4-2
4.1.1	Register Section .....	4-2
4.1.2	Arithmetic and Logical Unit .....	4-2
4.1.3	Interrupt Control .....	4-3
4.1.4	Timing and Control Unit .....	4-3
4.2	Basic Instruction Cycle .....	4-3
4.2.1	Interrupt Cycle .....	4-3
4.3	Instruction, Micro-instructions and Micro-operations Interpretation and Sequencing .....	4-5
4.3.1	Fetch Cycle .....	4-6
4.3.2	Execute Cycle .....	4-7
4.3.3	Interrupt Cycle .....	4-8
4.3.4	Examples of Microprograms .....	4-9
4.3.5	Applications of Microprogramming .....	4-12
4.4	Control Unit : Hardwired Control Unit Design Methods .....	4-12
4.4.1	State Table Method .....	4-13
4.4.2	Delay Element Method .....	4-13
4.4.3	Sequence Counter Method .....	4-14
4.4.4	PLA Method .....	4-14
4.5	Control Unit Soft Wired (Micro programmed) Control Unit Design Methods .....	4-14
4.5.1	Wilkie's Microprogrammed Control Unit .....	4-15
4.5.2	Comparison between Hardwired and Micro-programmed Control .....	4-16
4.6	Concepts of Nano Programming .....	4-16
•	Review Questions .....	4-16

**Module 5****Chapter 5 : Memory Organization      5-1 to 5-38**

**Syllabus :** Introduction and characteristics of memory, Types of RAM and ROM, Memory hierarchy, 2-level memory characteristic, Cache memory : Concept, Locality of reference, Design problems based on mapping techniques, Cache coherence and write policies, Interleaved and associative memory.

5.1	Introduction to Memory and Memory Parameters .....	5-2
5.1.1	Bytes and Bits .....	5-3
5.2	Memory Hierarchy : Classifications of Primary and Secondary Memories .....	5-4
5.3	Types of RAM and ROM .....	5-4
5.3.1	SRAM and DRAM .....	5-4
5.3.2	Types of Memory .....	5-5
5.3.2.1	Memory Map, Structure and its Requirements .....	5-5
5.3.3	Memory Chip Size and Numbers .....	5-6
5.4	ROM (Read Only Memory) .....	5-13
5.4.1	Types of ROM .....	5-13
5.4.2	Magnetic Memory .....	5-14
5.4.3	Optical Memory .....	5-16
5.5	Allocation Policies .....	5-18
5.6	Cache Memory : Concept, Architecture (L1, L2, L3) and Cache Consistency .....	5-20
5.6.1	Cache Operation .....	5-20
5.6.2	Principles of Locality of Reference .....	5-21
5.6.3	Cache Performance .....	5-21
5.6.4	Cache Architectures .....	5-22
5.6.5	Cache Consistency (Also Known as Cache Coherency) .....	5-23
5.6.6	Write Policy .....	5-23
5.6.7	Bus Master/Cache Interaction for Cache Coherency .....	5-25
5.6.8	Bus Snooping/Snarfing .....	5-26
5.6.9	Replacement Algorithms .....	5-26

5.6.10 Cost and Performance Measurement of Two Level Memory Hierarchy ..... 5-29

5.7	Cache Mapping Techniques .....	5-30
5.7.1	Direct Mapping Technique .....	5-30
5.7.2	Fully Associative Mapping .....	5-31
5.7.3	Set Associative Mapping .....	5-32
5.8	Interleaved and Associative Memory .....	5-33
5.8.1	Associative Memory .....	5-33
5.8.2	Interleaved Memory .....	5-33
5.9	Virtual Memory .....	5-35
5.9.1	Paging Mechanism or the Memory Management Unit .....	5-36
5.9.2	Segmentation .....	5-36
•	Review Questions .....	5-37

**Module 6****Chapter 6 : Principles of Advanced Processor and Buses      6-1 to 6-48**

**Syllabus :** Basic pipelined data path and control, Data dependencies, Data hazards, Branch hazards, Delayed branch and branch prediction, Performance measures - CPI, Speedup, Efficiency, Throughput, Amdhal's law, Flynn's classification, Introduction to multicore architecture, Introduction to buses : ISA, PCI, USB, Bus contention and arbitration.

6.1	Pipeline Processing .....	6-2
6.1.1	Non-Pipelined System Versus Two Stage Pipelining .....	6-2
6.1.2	Basic pipelined Datapath and Control for a Six Stage CPU Instruction Pipeline .....	6-3
6.1.3	Linear Pipeline Processors .....	6-4
6.1.3.1	Asynchronous and Synchronous Linear Pipelining .....	6-4
6.1.3.2	Clocking and Timing Control .....	6-5
6.1.3.3	Speedup, Efficiency and Throughput .....	6-6
6.1.4	Non Linear Pipeline Processors .....	6-7
6.1.4.1	Collision Free Scheduling or Job Sequencing .....	6-10



6.2 Instruction Pipelining and Pipelining Stages .....6-15	6.6 Introduction to Parallel Processing Concepts ....6-28
6.3 Pipeline Hazards .....6-16	6.6.1 Overlapping the CPU and Memory or I/O Operations .....6-28
6.3.1 Methods to Resolve the Data Hazards and Advances in Pipelining .....6-18	6.7 Flynn's Classifications .....6-28
6.3.1.1 Pipeline Stalls .....6-18	6.7.1 Flynn's Classification of Parallel Computing .....6-28
6.3.1.2 Operand Forwarding (or) Bypassing ....6-18	6.8 Superscalar Processors .....6-29
6.3.1.3 Dynamic Instruction Scheduling (or) Out-Of-Order (OOO) Execution .....6-19	6.8.1 Pipelining in Superscalar Processors ..6-29
6.3.2 Handling of Branch Instructions to Resolve Control Hazards .....6-19	6.9 Comparative Study of Multi-core Processors i3, i5 and i7 .....6-31
6.3.2.1 Pre-Fetch Target Instruction .....6-19	6.10 The ISA Bus .....6-32
6.3.2.2 Branch Target Buffer (BTB) .....6-19	6.10.1 8-bit ISA Bus .....6-32
6.3.2.3 Loop Buffer .....6-19	6.10.2 The 16-bit ISA Bus .....6-33
6.3.2.4 Branch Prediction .....6-19	6.10.3 The Extended ISA (EISA) Bus .....6-33
6.3.2.5 Pipeline Stall (Delayed Branch) .....6-20	6.10.4 The VESA (Video Electronics Standards Association) Local Bus .....6-33
6.3.2.6 Loop Unrolling Technique .....6-20	6.10.5 Applications if ISA Bus .....6-33
6.3.2.7 Software Scheduling or Software Pipelining .....6-20	6.10.6 ISA Timers .....6-34
6.3.2.8 Trace Scheduling .....6-21	6.11 The Peripheral Component Interconnect (PCI) Bus .....6-34
6.3.2.9 Predicated Execution .....6-22	6.11.1 Features of PCI Bus .....6-35
6.3.2.10 Speculative Loading .....6-23	6.11.2 Configuration Space of PCI Card.....6-36
6.3.2.11 Register Tagging .....6-23	6.11.3 PCI Interface with the Processor .....6-37
6.3.3 Branch Prediction .....6-23	6.11.4 Classification or Variants of PCI Bus ...6-38
6.3.3.1 Misprediction Penalty .....6-23	6.11.5 Applications of PCI Bus .....6-38
6.3.3.2 Static Branch Prediction .....6-23	6.11.6 BIOS for PCI .....6-38
6.3.3.3 Branch-Target Buffer or Branch-Target Address Cache .....6-24	6.12 The Universal Serial Bus (USB) .....6-40
6.3.3.4 Dynamic Branch Prediction .....6-24	6.12.1 Features of USB .....6-40
6.3.3.5 One-bit Dynamic Branch Predictor .....6-24	6.12.2 Classification of USB .....6-42
6.3.3.6 Two-bit Prediction .....6-24	6.12.3 Applications of USB .....6-42
6.4 Performance Measures of Computer Architecture .....6-24	6.12.4 USB Transfers .....6-42
6.5 Principles of Scalable Performance .....6-26	6.12.5 USB Commands .....6-43
6.5.1 Amdahl's Law .....6-26	6.13 Bus Contention and Arbitration .....6-44
6.5.2 Gustafson's Law .....6-27	6.13.1 Bus Arbitration .....6-45
	• <b>Review Questions</b> .....6-47
	• <b>Appendix-A : Shift Registers</b> ..... A-1 to A-12